REMARKS

Claims 1-20 are pending in this application, of which claims 1, 8, and 16 are independent. Favorable reconsideration and further examination are respectfully requested.

All of the claims were rejected over U.S. Patent No. 5,339,275 (Hyatt). As shown above, the claims have been amended. For example, claim 1 now recites an error signal generator to generate an error signal and to provide the error signal to the control circuit such that the error signal is applied to a signal on the forward path of the control circuit, that the error signal is predetermined, and that the error signal generator is external to the control circuit.

Page 3 of the Office Action states the following regarding the error generator:

> an error signal generator to generate an error signal and to provide the error signal to the control circuit (see Col. 92, Line 59 to Col. 93, Line17), wherein the forward path is configured to generate an output signal based on the sensor signal and the error signal (see Col. 92, Line 59 to Col. 93, Line17), the output signal being sent along the feedback path to the input of the forward path (see Col. 92, Line 59 to Col. 93, Line17); and

The cited portion of Hyatt is reproduced below, along with the figure (11F) that it references.

> For simplicity of discussion, an OTA servo arrangement is provided for scale factor compensation. This arrangement is merely exemplary of other servo arrangements and other scale factor arrangements which can be implemented by those skilled in the art from the teachings herein. Servo 1113 comprises OTA 1116 for amplifying the sampled signal from sample-and-hold circuit 961A. The sampled signal is compared with reference signal V_{REF} using differential amplifier 1117 for generating a feedback error signal to OTA gain controlling input I_{ABC}. Servo 1113 is connected so that a deviation of the amplified sampled signal from the V_{REF} signal is indicative of an amplitude error condition. The output signal from differential amplifier 1117 is a servo error signal which is fedback to control the gain of OTA 1116 with the amplifier bias current (ABC) I_{ABC} to adjust the output signal from OTA 1116 to the amplitude of reference signal V_{REF}. Gain controlling current I_{ABC} is also used to compensate the memory output signal 936 by controlling gain or OTA 1114 with signal 1115 to OTA gain control input I_{ABC} to compensate for scale factor errors in memory output signal 936, generating compensated output signal 960. The I_{ABC} current

signal to OTAs 1114 and 1116 can be generated by well known current generators such as with well known current sources; shown functionally as differential amplifier 1117.[1]

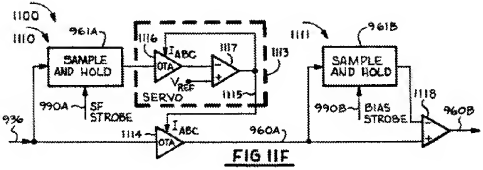

FIG 11E

As is evident from the excerpt and figure above, the error signal – here the feedback signal from 1117 to 1116 – is not applied to a signal on the forward path of the control circuit. Rather, in Hyatt, the error signal is used to control the gain of amplifiers (OTAs) 1116 and 1114. Moreover, the error signal in Hyatt is not a predetermined signal. Rather, in Hyatt, the error signal corresponds to "deviation of the amplified sampled signal from the V_{REF} signal"[2]. In other words, the error signal is not predetermined in the sense that it is part of the feedforward path, i.e., the error signal is dependent on the output of OTA 1116.

Furthermore, we note that the Office Action equates circuit 996 of Fig. 9 to the claimed control circuit.[3] However, as explained in the following excerpts, the circuitry of Figs. 11 constitutes alternative implementations of the circuitry of Figs. 9.

> The adaptive compensation feature of the present invention will now be exemplified with an alternate memory embodiment shown in FIG. 11. Because similar arrangements have already been discussed such as with reference to the arrangements shown in FIGS. 9F to 9T, the arrangements shown in FIG. 11 will now be discussed in simplified form. For example, differential amplifier 976 and gain control amplifier 963 are shown in FIG. 9 having input resistors and feedback resistors, but for simplicity of illustration, gain control amplifier 1114 and differential amplifier 1118 are shown in FIG. 11 without resistors. The use of resistors for amplifiers 1114 and 1118

[1] Col. 92, line 59 to col. 93, line 17
[2] Col. 93, lines 1 and 2
[3] Office Action, page 3

shown in FIG. 11 will become obvious from the discussions of FIG. 9, wherein resistors may be considered to be included in gain controlled amplifier 1114 and differential amplifier 1118. (emphasis added)

As discussed with reference to FIG. 9, various forms of compensation may be used either separately or in combinations. Compensation may include scale factor compensation, bias compensation, and other forms of compensation. For simplicity of discussion, scale factor compensation and bias compensation will be discussed in various combinations and configurations relative to FIG. 11 to exemplify the more general features of the present invention. Memory signal compensation arrangement 1100 is shown in FIG. 11 having various alternate compensation configurations.[4]

Thus, the alleged error signal generator of Fig. 11 (col. 92, line 59 to col. 93, line 17) is actually part of the alleged control circuit of Fig. 9 (circuit 996). By contrast, claim 1 requires that the error signal generator be external to the control circuit.

The Office Action also states the following regarding error signal generation

As to dependent claim 12, Hyatt teaches the method of claim 10, further comprising:

generating an error signal based on an output of a time signal generator and an output of the decision logic (see Col. 87, Lines 56-62); and

applying the error signal to the forward path, the intermediate signal being based on both the sensor signal and the error signal (see Col. 19, Lines 35-43).

The cited portion of column 87 reads as follows:

Because many error mechanisms are time related such as thermally generated leakage, shifting operations such as recirculation may be implemented as relatively high-speed operations. Also, because access time is related to shift rate, shifting operations such as recirculation may be implemented as relatively high-speed operations. Alternately, output operations such as for A/D conversion in a hybrid memory embodiment, or interfacing to a slower speed serial data channel, etc may require a lower output rate. For example, in the hybrid memory embodiment, refresh and recirculation may be relatively higher speed operations while A/D conversion may be a relatively lower speed operation.[5]

[4] Col. 91, lines 41 to 68
[5] Col. 87, lines 56 to 62

This portion of Hyatt merely describes implementing certain operations, such as recirculation, at high speeds, apparently in order to address errors. However, this portion of Hyatt is not understood to disclose or to suggest the foregoing features of amended claim 1.

The cited portion of column 19 reads as follows:

> Input signals 504 and 505 and output signals 506 and 507 may be interconnected for feedforward and/or feedback operations. For example, an output signal 506 having a first time delay may be connected to an input signal 505 having a second time delay. If the first time delay is greater than the second time delay, then a feedback connection is provided. If the second time delay is greater than the first time delay, then a feedforward connection is provided.[6]

This portion of Hyatt describes connecting signals based on time delays. We do not see how this portion of column 19 relates to column 87. That is, the rejection states:

> **As to dependent claim 12**, Hyatt teaches the method of claim 10, further comprising:
>
> generating an error signal based on an output of a time signal generator and an output of the decision logic (see Col. 87, Lines 56-62); and
>
> applying the error signal to the forward path, the intermediate signal being based on both the sensor signal and the error signal (see Col. 19, Lines 35-43).

Since former claim 12 recites applying "the" error signal, it means that the error signal generated by column 87 is "applied". That does not appear to be the case here. In any case, the cited portions of claim 19 and 87, taken alone or in combination, are not understood to disclose or to suggest the foregoing features of amended claim 1.

For at least the foregoing reasons, claim 1 is believed to be patentable. Independent claims 8 and 16 are likewise believed to be patentable.

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[6] Col. 19, lines 35 to 43

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing remarks, the entire application is now believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please apply any deficiency in fees or credit any overpayment to deposit account 06-1050, referencing Attorney Docket No. 14603-013US1.

Respectfully submitted,

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